REMARKS

Claim 9 is rejected under 35 USC 112, second paragraph, as being indefinite because claim 9 should be dependent upon claim 8.

Applicant has amended claim 9 to be dependent upon claim 8 as was suggested by the Examiner. No new matter is entered.

Claims 1-2, 5, 6-7, 10 are rejected under USC 102e as being anticipated by Chen et al. (US Pat#6,993,618)

Applicant has amended claim 1 to include all the limitations of claim 5 and to additionally include the features "transferring data stored on the first peripheral device to the second peripheral device according to a command from the host but without buffering the data in the host and without transferring the data through the SATA port". (newly claimed features underlined) Claim 5 is correspondingly cancelled. Similar amendments are made to independent claim 6. Claim 10, having being incorporated into claim 6, is correspondingly cancelled.

No new matter is entered by the above described amendments. In particular, applicant notes that paragraph [0021] of the original specification as filed states, "The CPU 504 controls the first, second, third peripheral devices 402, 404, 406 according to commands from the host 408 using the optical storage control 508, flashcard control 510, or other device control 512, respectively, which are connected to the first, second, third peripheral devices 402, 404, 406 using the digital means 422"; and paragraph [0022] of the original specification as filed states, "The data does not need to be sent across the SATA interface to be temporarily buffered in the host 408."

Concerning the rejection of original claims 5 and 10, the Examiner stated in the Office action dated 02/15/2007 that "the peripheral devices include a first peripheral device (F.2 flash memory 26) and a second peripheral device (F.2 flash memory 32), and the controller directly transfers data stored on the first peripheral device to the second peripheral device

without buffering the data in the host (col. 2 lines 60-67)." However, applicant notes that Chen et al. do not teach directly transferring data between first peripheral device (F.2 flash memory 26) and a second peripheral device (F.2 flash memory 32). In fact, Chen et al. state in col 4. lines 4-5, "Usually only one of compact-flash card 22, smart-media flash-card 26, secure-digital/multi-media card 32, and memory stick interface 34 is plugged in at a time." Instead, Chen et al. teach transferring data from one of the four memory cards 22, 26, 32, or 36 to the USB flash memory (key drive) 16. According to the Examiner's rejection, the USB interface 18 is substituted with a SATA interface. In this way, applicant notes that doing a direct DMA transfer of data from one of the peripheral devices 22, 26, 32, or 36 to the flash memory key drive 16 is not equivalent to the present invention as claimed in currently amended claim 1 because according to Chen et al. the data needs to pass through the SATA interface 18 in order to be stored in the flash memory key drive 16.

Applicant also notes that it is impossible for the USB dual-mode microcontroller 30 to directly transfer the data from one of the peripheral devices 22, 26, 32, or 36 into the flash memory key drive 16 according to a command from the host PC 10. The reason is that when the host PC 10 is coupled to the dual mode microcontroller 30, the dual mode microcontroller 30 must operate as a USB peripheral controller (slave) in order to be able to receive and act according to commands from the host 10. However, this also means it will not be able to act as a master in order to send data and information directly to the flash memory drive key 16, which will also be acting as a USB peripheral controller (slave) since that is the only functionality it includes. See col 3, lines 48-57 stating, "USB dual-mode microcontroller 30 can operate as a USB peripheral controller (slave) or as a USB host controller (master). USB bus 18 is the upstream USB bus segment when host PC 10 is connected through USB connector 12, but acts as a downstream USB bus segment when host PC 10 is not connected. When USB-memory key drive 16 is plugged into USB connector 17, USB dual-mode microcontroller 30 can send USB packets downstream over USB bus 18." This is why the microcontroller 30 is labeled as a dual-mode microcontroller 30 by Chen et al. (emphasis added) It operates as the master when the host 10 is not connected or operates as a slave when

the host 10 is connected.

In this way, the dual-mode microcontroller 30 needs to operate in host mode in order to transfer data to the drive key 16, but the dual-mode microcontroller 30 can only operate in host mode when the host 10 is NOT connected to the microcontroller 30. Therefore, applicant asserts it is impossible for the dual-mode microcontroller 30 of Chen et al. to directly transfer data to the flash memory drive key 16 according to a command from the host 10 but without buffering the data in the host 10.

Additionally, applicant has reviewed the further teachings of the reference of Chen et al. and notes that Chen et al. also teaches flash integrated memory module 42, which as described in col. 4, lines 42-49, "USB dual-mode microcontroller 30 may transfer data from compact-flash card 22 to flash-integrated memory module 42 when host PC 10 and USB-memory key drive 16 are not connected." (emphasis added) Applicant notes that although such transfer of data to the flash integrated memory module 42 does not require the data to cross the SATA interface 18, such transfer is not in response to a command from the host 10 because the host PC 10 is not connected. Therefore such operation is also not equivalent to the present invention as claimed in currently amended claim 1 because the direct transfer does not occur according to a command from the host 10. Also, note that Chen et al. teach in column 6, lines 51-58, "When the host PC is not connected, step 115, and USB-memory key drive 16 is also not connected, step 118, then data cannot be transferred. An error is signaled by blinking the USB-memory key LED. The LED can blink red or yellow rather than green to indicate the error. If flash-integrated memory module 42 is present, transfer could occur to the internal flash-integrated memory module using the local host mode (not shown)." (emphasis added) Applicant again notes that such data transfer to the flash integrated memory module 42 cannot be according to a command from the host PC 10 because the host 10 is not connected to the SATA interface 18 at this time. Additionally, applicant again notes that the dual-mode microcontroller 30 only operates in local host mode when the host PC 10 is not connected, and therefore the dual-mode microcontroller 30 cannot perform operations according to commands from the host PC 10 while operating in local host

mode. (Since local host mode is only utilized when the host 10 is not connected.)

Concerning the reference of Bissessur et al. also cited by the Examiner, applicant further asserts that currently amended claims 1 and 6 should not be found obvious in view of Chen et al., and further in view of Bissessur et al. because said references do not fairly teach or suggest, either alone or in combination, all the features of the present invention as claimed in currently amended claims 1 and 6. In particular, applicant notes that Bissessur et al. also do not teach directly transferring data from one disk 60a to another disk 60n without transferring the data through the SATA port, as is claimed in the present invention claims 1 and 6. The reason is that when the controller 54 is a SATA controller, the disks 60a and 60n shown in Fig.2 of Bissessur et al. will clearly be SATA disks. See paragraph [0023] of Bissessur et al. stating, "in embodiments where the disk controller 54 comprises a SATA controller". Applicant notes that therefore the interface (indicated as solid lines in Fig.2 for example) between the disks 60a and 60n to the SATA controller 54 is a SATA interface being controller by the SATA controller 54 - not a digital means as is claimed in the present invention. Therefore, the data transferred from one disk 60a to another disk 60n by the SATA controller 54 must be transferred through the SATA port according to the teachings of Bissessur et al.. Such operation is in contrast to the present invention as claimed in currently amended claims 1 and 6.

For at least the above-described reasons, applicant asserts that currently amended independent claim 1 should be found allowable with respect to the teachings of Chen et al. A similar argument also applies to currently amended independent claim 6. Claims 2-4 and 7-9 are dependent upon claims 1 and 6, respectively, and should therefore also be found allowable for at least the same reasons as their respective base claims. Reconsideration of claims 1-4 and 6-9 is respectively requested.

Claim 3-4, 8-9 are rejected under 35 USC 103a as being unpatentable over Chen et al.

(US Pat#6,993,618), in view of Bissessur et al. (US Pub# 2004/0019713)

As previously mentioned, claims 3-4, 8-9 are dependent upon claims 1 and 6, respectively. Therefore claims 3-4, 8-9 are believed allowable by the applicant for at least the same reasons provided above for claims 1 and 6. Withdrawal of the 35 USC 103a rejection of claims 3-4, 8-9 is respectfully requested.

Additionally, applicant has amended claim 3 to state, "wherein the peripheral devices electrically coupled to the controller simultaneously comprise an optical storage device and a non-volatile storage device." (newly claimed feature underlined) A similar amendment is made to claim 8. No new matter is entered. For example, please refer to Fig.4 of the present invention and paragraph [0020] stating, "in FIG. 4, the first peripheral device 402 is an optical storage device and includes an optical pick-up 415, and an optical medium 416. The second peripheral device 404 is a flash card device and includes a flash card access device 418."

Applicant points out that neither Chen et al. nor Bessessur et al. teach simultaneously attaching an optical storage device and a non-volatile storage device as peripheral devices to the controller combined with the other features as claimed in claims 1 and 6. For at least this reason, applicant asserts that claims 3 and 8 should be found allowable with respect to the cited references. Claims 4 and 9 are dependent claims and should be found allowable for at least the same reasons. Reconsideration of claims 3-4 and 8-9 is respectfully requested.

Conclusion

Thus, all pending claims are submitted to be in condition for allowance with respect to the cited art for at least the reasons presented above. The Examiner is encouraged to telephone the undersigned if there are informalities that can be resolved in a phone conversation, or if the Examiner has any ideas or suggestions for further advancing the prosecution of this case.

Sincerely yours,

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